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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,727	03/09/2004	Larry L. Byers	MP0787	1768

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EXAMINER	
THOMAS, SHANE M	
ART UNIT	**PAPER NUMBER**
2186	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/796,727	BYERS ET AL.	
	Examiner	Art Unit	
	Shane M. Thomas	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 9-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 9-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/4/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office action is responsive to the application filed 3/9/2004. Claims 1-7 and 9-25 are presented for examination and are currently pending.

In the response to this Office action, the Examiner politely requests that support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line numbers in the specification and/or drawing figure(s). This will assist the Examiner in prosecuting this application.

Excerpts from all prior art references cited in this Office action shall use the shorthand notation of [column # / lines A-B] to denote the location of a specific citation. For example, a citation present on column 2, lines 1-6, of a reference shall herein be denoted as "[2/1-6]."

Priority

Priority from provisional application 60/453,241 is acknowledged.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 4/4/2005 has been considered by the Examiner. It is noted that the non-patent reference "Computer Architecture and Parallel Processing" (pp 156-164) has been considered despite photo-copying error evidenced on the bottom portion of the supplied reference. The Examiner has only considered the legible portion of the reference included therewith.

Specification

The disclosure is objected to because of the following informalities:

(1) the Docket Numbers of each of the Cross Referenced Applications (pages 1-2 of the specification) should be removed; and

(2) the updated figure numbers of the drawings filed on 6/7/2004 should be reflected in the "Brief Description of the Drawings" section of the specification.

Appropriate correction is required.

Claim Objections

Regarding claim numbering, it appears that claim 8 as been mistaken omitted.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 7,9,20, and 21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

As per claims 7,9,20, and 21, Applicant's specification as originally filed has not enabled the terms "hard semaphore" and "soft semaphore." The only mention of these two elements throughout the specification occur in the sections of the "Abstract" and the "Summary of the Invention," which is merely a recitation of the claims themselves. The term "hard semaphore" and "soft semaphore" are not terms of art, as a search of the terms did not yield a common definition, respectively. Additionally, a definition for the terms cannot be found in the "IEEE Dictionary of Standard Terms" nor the "Microsoft Computer Dictionary."

Further, the Examiner has consulted the priority document (60/453,241) for the definition. Page 1 of the provisional application defines the terms; however, a clear definition has not been supplied to adequately distinguish a "hard semaphore" from a "soft semaphore." Applicant defines a "hardware semaphore" as "a hardware mechanism that insures indivisible register read/update/write sequence that may be performed by the first main processor or the second processor using firmware," while defining a "software semaphore" as "a mechanism that insures indivisible register read/update/write sequence that may be performed by the first main processor or the second processor using firmware." Therefore, as defined, it appears that the "hardware semaphore" is merely a subset of "software semaphores." For the purposes of expedited prosecution of this application, the Examiner has considered the term "hardware semaphore" in line with the provisional application in that the semaphore is included in an element of hardware and that the "software semaphore" is any semaphore (including those maintained in hardware).

Claims 10 and 22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 10 and 22, it is not clear to which "transactions" the terms "the first and second processor transactions" are referring as the term lacks antecedent basis. Nonetheless, for the purposes of examination, the Examiner has considered the term "first and second processor transactions" to be processor transactions used to attempt to gain control of a shared resource.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1,3-6,10-12,14,16-19, and 22-24, are rejected under 35 U.S.C. 102(e) as being anticipated by Gary et al. (U.S. Patent No. 6,662,253).

As per claims 1 and 14, Gary teaches an embedded disk controller (figure 1 sans elements 101 and 107) having a servo controller (combination of elements 105 and 108), comprising:

A servo controller interface (combination of all elements within element 103 and element 104 of figure 1 *except* servo controller (elements 105 and 108)) with a speed-matching module 104 [3/48-51] and a pipeline control module 205 (shown in figures 2 and 3) such that at least two processors (P0 110 and P1 111) share memory mapped registers without conflicts [4/65 - 5/13]

and [5/29-49]. Gary teaches in section [4/65 - 5/13] that peripheral devices are shared among the processors P1 and P0, wherein each device is memory mapped to a designated address space, and wherein that range of memory mapped addresses includes identification for registers. Therefore, it can be see that because the processors share the peripheral devices without conflict and each device has its own registers that are memory-mapped, that the processors share the memory mapped registers without conflicts. The pipeline control module 205 serializes access to the devices to one processor at a time as discussed in [5/29-49].

As per claims 3 and 16, it is necessarily inherent that the bus element connecting the servo controller interface (defined supra) to the servo controller (also defined supra) operates at a given frequency. As such, claims 3 and 16 are anticipated since the claim only states that the servo controller and the servo controller interface must operate in the same or different frequency domains. Since the controller and the interface are in operation together (as the disk controller 103 of Gary can used to access a disk medium 107) it is necessarily inherent that they are operating either in the same frequency domain or different frequency domains.

As per claims 4 and 17, Gary teaches [3/45-51] that the speed matching module 104 ensures communication between the host and the disk controller 103 without inserting wait states to the servo controller interface when writing to the servo controller. In other words, because of the difference in frequency domains in which the disk drive and host operate, all incoming write data is buffered in the speed-matching module 104 before being written to the hard drive 107. The write can then be supplied to the disk drive 107 via the servo controller (105+108) from the servo controller interface (defined supra) without the servo controller interface inserting wait states (between write data). Essentially (as known in the art) the speed-matching module allows

the servo controller to find the location of the data that is to be written and then supplies the data to the servo interface to be written to the disk drive. This process repeats with the speed-matching module reading the data for next location of data to be written while the servo controller reads the disk drive to that data location. Then once the location has been accessed, the data is supplied from the interface to the controller (105+108); thereby preventing wait states or having the servo controller interface *itself* wait for the data from the host 101 while the controller rotates the disc heads to the proper location on the disk.

As per claims 5 and 18, because the pipeline control module 205, the processors exclusively share access to the disk drive 107 [6/55-67], and a situation cannot arise where both processors are reading from the disk drive at the same time (i.e. read conflict).

As per claims 6 and 19, the pipeline control module 205 comprises a hardware mechanism for indivisible register access [7/7-15] to the first or second processor. In other words, only one processor may be the owner of the peripheral's I/O register 301 (figure 1), thereby being able to access the peripheral [5/23-27].

As per claims 10 and 22, the pipeline control module 205 resolves conflict (simultaneous access request from both processors for the same resource) between the first and second processor transactions (for access control) [6/48-54] - the protocol logic 204 of the pipeline control module 205 (figure 1) implements the dynamic sharing of the peripherals with the processors.

As per claims 11 and 23, as shown in figure 1, the first and second processor communicate with the servo controller via separate buses (both labeled 102) - [4/2-3].

As per claims 12 and 24, assuming processor P1 is the owner of a given peripheral (in this case the disk drive 107 itself), the pipeline control module 205 will hold write access to the second processor P0 until the first processor releases the peripheral from its ownership - [6/55 - 7/6].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 and 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Gary et al. (U.S. Patent No. 6,662,253).

As per claims 2 and 15, the Examiner is taking OFFICAL NOTICE with regards to one processor operating at a first frequency and a second processor operating at a second frequency as it is well known in the art that processors may operate at unique frequencies. Gary teaches in [3/63-65] that the processors P0 and P1 may be different to optimize particular tasks. Therefore, it would have been obvious to one having ordinary skill in the art to have modified the disk controller of Gary in order to have used different processor frequencies to optimize the desired performance for the specific desired tasks.

Claims 7,9,13,20,21, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gary et al. (U.S. Patent No. 6,662,253) in view of Snyder et al. (U.S. Patent No. 6,745,274).

As per claims 7,9,20, and 21, Gary suggests the need for a processor that loses a race condition when vying for a common resource to be made aware that it failed to acquire the resource (to be able to reschedule the write data in one example presented by Gary) but does not specifically teach using a semaphore to control sharing access of the common resource. Snyder teaches a semaphore to synchronize access to a shared resource [1/22-25] and [2/26-38] without requiring special instructions to implement the synchronization control [8/31-36]. Further, Snyder teaches in [4/37-40] that the use of the semaphore allows for processor that did not successfully acquire the shared resource to "learn of the failure" and re-attempt to acquire the semaphore lock - thereby providing a resolution to the suggestion of Gary - [7/11-15].

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have combined the disk controller system of Gary with the teaching of a semaphore of Snyder in order to have implemented a sharing technique that would have allowed a processor (p0, p1) of the system of Gary to have determined that it lost or did not acquire a shared resource when both processors simultaneously request access to the shared peripheral. Once the determination is made, the losing processor may vie for the semaphore lock again to access the peripheral once the other processor releases the lock (figure 2, step 200 of Snyder).

Regarding claims 7 and 20, the semaphore is being considered by the Examiner to be a "hardware semaphore" as the semaphore is taught by Snyder as comprising hardware components (i.e. registers - [2/20-21]).

Regarding claims 9 and 21, as the definition for a software semaphore is not distinguished from a hardware semaphore (see the argument posed above with regard to the §112, 1st paragraph, section), the rejection for claims 7 and 20 is applied to claims 9 and 21 as well.

As per claims 13 and 25, Snyder teaches that the hardware mechanism of the disk controller system of modified Gary can be a semaphore register [2/20-21].

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Alexander et al. (U.S. Patent No. 6,467,006) teaches that controller processors that vie for a shared resource may have varying differences in clock frequencies.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane M Thomas whose telephone number is (571) 272-4188. The examiner can normally be reached M-F 8:30 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt M Kim can be reached at (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane M. Thomas

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